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Low-Voltage Organic Field-Effect Transistors (OFETs) with Solution-Processed Metal-Oxide as Gate Dielectric

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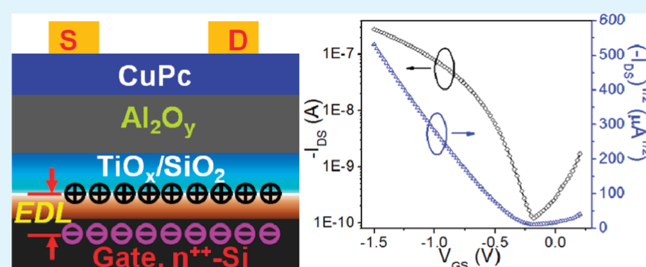
S Supporting Information

ABSTRACT: In this study, low-voltage copper phthalocyanine (CuPc)-based organic field-effect transistors (OFETs) are demonstrated utilizing solution-processed bilayer high-*k* metal-oxide (Al_2O_y/TiO_x) as gate dielectric. The high-*k* metal-oxide bilayer is fabricated at low temperatures (< 200 °C) by a simple spin-coating technology and can be controlled as thin as 45 nm. The bilayer system exhibits a low leakage current density of less than 10^{-5} A/cm^2 under bias voltage of 2 V, a very smooth surface with RMS of about 0.22 nm and an equivalent *k* value of 13.3. The obtained low-voltage CuPc based OFETs show high electric performance with high hole mobility of 0.06 cm^2/(V s), threshold voltage of −0.5 V, on/off ration of 2 × 10^3 and a very small subthreshold slope of 160 mV/dec when operated at −1.5 V. Our study demonstrates a simple and robust approach that could be used to achieve low-voltage operation with solution-processed technique.



KEYWORDS: low-voltage, OFETs, solution-processed, high-*k*, Al_2O_y/TiO_x, CuPc

INTRODUCTION

A great deal of research interest has been devoted to organic field-effect transistors (OFETs) during the past decades, as they have many advantages such as light weight, flexibility, and low temperature and solution processability.[1] Much progress has been made in improving the performance of OFETs; however, high operation voltage resulting from intrinsically low charge carrier mobility of organic semiconductors remains a severe limitation that hinders their development in practical applications.[2] For low-power applications, such as RFID tags, flat panel displayers, and portable electronics, it is a prerequisite to achieve high FET performance at acceptably low voltage. Typically, this issue can be addressed through increasing the capacitance density of the gate dielectrics (C_i) by means of either increasing the dielectric constant (k) or decreasing the thickness (d) ($C_i = \varepsilon_0 k/d$). The latter approach has been demonstrated by utilizing self-assembled monolayers (SAMs) and multilayers (SAMTs),[3−5] as well as polymers.[6,7] However, because of the low dielectric constants (typically <3) of organic materials, an extremely thin dielectric thickness is required. This demands a particularly careful preparation of the dielectric layer (as a very small amount of defects can already cause high leakage current) and makes the scale-up of OFET fabrication difficult.

Application of high-*k* inorganic metal-oxides, such as TiO_2, HfO_2, ZrO_2 and Al_2O_3, instead of organic dielectrics, offers a promising alternative. Among these binary metal-oxides, TiO_2 is known to have the highest *k* value, but has the disadvantage of a negligible band offset against Si[8] and the easy formation of an interface layer even at low temperature.[9] Moreover, a higher permittivity value is usually accompanied by a smaller band gap, resulting in larger leakage currents through the gate dielectric. On the other hand, HfO_2 and ZrO_2 tend to form polycrystalline phases at relatively low temperature, resulting in the formation of grain boundaries that will degrade the dielectric performances.[10] In comparison, the merits of Al_2O_3 are its large band gap and band offset with Si[8] and excellent thermal stability.[11] Although the *k* value of Al_2O_3 is moderate, it can be used in combination with TiO_2 considering the fact that they have characteristics complementary to each other. On the other hand, typical processing routes for metal-oxide dielectrics, including chemical vapor deposition (CVD),[12] atomic layer deposition (ALD)[13] and radio-frequency (rf) magnetron sputtering[14] are often associated with high temperature, require expensive, high vacuum equipment, and are time consuming to produce. To achieve roll-to-roll metal-oxide fabrication and to make it compatible with large area flexible substrates, it is crucial to develop low-temperature, solution-processed routings for the fabrication of metal-oxides as gate dielectrics.

In this paper, we describe a novel solution-processed method to fabricate a 45 nm thick, bilayer Al_2O_y/TiO_x dielectric system at low temperature (200 °C). The obtained dielectric system exhibits a very smooth surface (RMS = 0.22 nm), a low leakage current density (1 × 10^{-5} A/cm^2), and a high capacitance

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density of 250 nF/cm^2. By applying such a system as the gate dielectric, we achieve high performance of copper phthalocyanine (CuPc) based OFETs at a driving voltage as low as -1.5 V, and the hole mobility (μ), threshold voltage (V_T), on/off ratio, and subthreshold swing (SS) are determined to be 0.06 cm^2/(V s), -0.5 V, 2×10^3, and 160 mV/dec, respectively. Our approach demonstrates a low-temperature, scalable process for fabrication of high-capacitance gate dielectric, which is a key step towards the realization of low-voltage OFET circuits.

EXPERIMENTAL SECTION

Titanium oxide (TiO_x) sol was prepared by dissolving titanium(IV) isopropoxide (TIP) ($Ti(OC_3H_7)_4$, 99.99%, Aldrich) into a mixture of methanol and acetic acid in a concentration of about 0.1 mol/L, and then vigorously stirred for 24 h in ambient conditions. Aluminum oxide (Al_2O_y) sol was prepared by dissolving aluminum nitrate nonahydrate ($Al(NO_3)_3 \cdot 9H_2O$, 99.99%, Aldrich) into 2-methoxylethanol in a concentration of about 0.5 mol/L and then stirred for 12 h in ambient conditions.

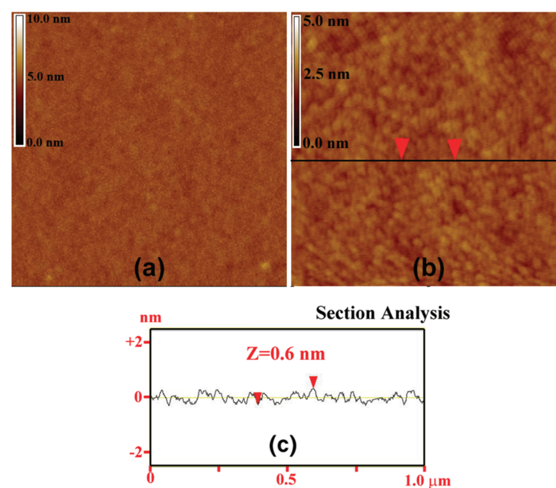
Prior to dielectric layer deposition, heavily n-doped Si wafers (n^{++}-Si) (acting as gate electrodes) were ultrasonically cleaned by acetone, isopropanol and ethanol, in succession, and then used immediately for spin-coating after blown dry with N_2 gas. The TiO_x layer was deposited by spin-coating the TiO_x sol onto the cleaned n^{++}-Si substrates at 5000 r/min for 40 s, followed by baking at 200 $\pm$ 5 °C for 5 min to ensure the hydrolyzation and decomposition of the precursor. Subsequently, the Al_2O_y layer was deposited by spin-coating the Al_2O_y sol onto the cooled TiO_x-coated substrates and then baked at the same condition as that of TiO_x.

After deposition of the dielectric layers, bottom gate, top contact (BGTC) OFETs were fabricated by vacuum deposition of CuPc (30 nm, 3×10^{-4} Pa, 0.01 nm/s growth rate) onto the substrates at the substrate temperature of 180 °C, followed by vacuum deposition of gold as source (S)−drain (D) electrodes (30 nm, 3×10^{-4} Pa, 0.03 nm/s growth rate) through a shadow mask with dimensions of L (channel length) = 70 μm and W (channel width) = 2500 μm. As for leakage and capacitance characterization, a metal-insulator-metal (MIM) structure was fabricated by direct deposition of 30 nm thick gold dots with diameter of 1000 μm onto the single layer TiO_x and bilayer Al_2O_y/TiO_x dielectric system through a shadow mask. For comparison, n^{++}-Si wafers with thermally grown 300 nm SiO_2 layer were also cleaned under the same procedures, and directly used for fabrication of OFETs under the same conditions as that of bilayer Al_2O_y/TiO_x.

The surface morphology of the solution-processed dielectric and CuPc film was characterized by atomic force microscopy (AFM, Nanoscope IIIa Vecco) in tapping mode. The elemental analysis of the spin-coated metal-oxides were characterized by XPS spectrometer (VG Scientific ESCALAB 250, equipped with two ultra-high-vacuum (UHV) chambers) measurements and all binding energies were referenced to the C 1s peak at 284.6 eV of the surface adventitious carbon, the depth profiling was performed by Ar^+ etching with an EX05 argon gun at ion beam voltage of 3 keV and emission current of 2 μA. The frequency-dependent capacitance of the MIM structure was measured by HP 4284A in a frequency range of 1k Hz to 1M Hz. The electronic characteristics of the OFETs were measured in ambient conditions using Keithley 4200 SCS.

RESULTS AND DISCUSSION

The X-ray diffraction (XRD) characterization is conducted on the solution-processed single-layer TiO_x and bilayer Al_2O_y/TiO_x system. The absence of diffraction peaks in the XRD patterns reveals the amorphous nature of the oxides obtained at low



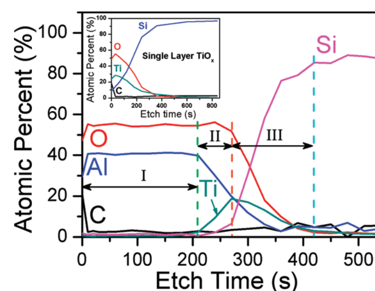


Figure 1. AFM images of bilayer Al_2O_y/TiO_x in an area of (a) 5 μm × 5 μm and (b) 1 μm × 1 μm, and (c) cross-sectional height profile obtained from the black solid line in b.

Figure 2. Atomic composition profile for Al, O, Ti, Si, and C of bilayer Al_2O_y/TiO_x system as a function of etching time; inset: Atomic composition profile for Ti, O, C, and Si of single-layer TiO_x.

processing temperature (200 °C) (see Figure S1 in the Supporting Information). Figure 1a shows the tapping mode AFM image of the bilayer Al_2O_y/TiO_x system. As seen, the bilayer Al_2O_y/TiO_x exhibits a homogenous and smooth surface with a root mean square (RMS) roughness value of ~0.22 nm in an area of 5 μm × 5 μm, as smooth as that of the n^{++}-Si substrate with 300 nm SiO_2 (RMS ~0.19 nm). In addition, as shown in Figure 1b, no surface defects and pinholes are observed in the higher resolution AFM image. The section analysis along a scan line (Figure 1c) further confirms the high quality of the solution-processed film with a surface height fluctuation within 0.6 nm. The single TiO_x layer (AFM image not shown here) also shows similar structure, and has a considerably lower roughness than the reported TiO_2 dielectric layer which is obtained from a sol-gel and has a roughness value of 4 nm.[15] The dielectric surface roughness is an important factor that can influence the performance of OFETs. A rough dielectric surface has been proved to be harmful to charge carrier transport in organic semiconductors. It can induce physical traps and barriers,[16] or disturb the growth of the semiconductor layer.[17] Therefore, the smooth surface of our bilayer Al_2O_y/TiO_x system is an ideal property for high-performance OFETs.

To investigate the chemical structure of the spin-coated dielectric films, we conducted XPS measurements. Figure 2 shows the atomic composition profiles of O, Al, C, Ti, and Si as

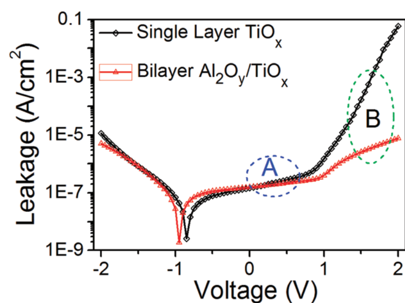


Figure 3. Leakage current density versus bias voltage characteristics of MIM structures.

a function of etching time obtained from the bilayer Al_2O_y/TiO_x system. We note that no N atom is detected in the film, indicating completely decomposition of Al precursor ($Al(NO_3)_3 \cdot 9H_2O$). As can be seen in region I, the stoichiometry of the top Al_2O_y layer remains unchanged throughout the thickness of the layer, and no Si and Ti are detected in this region. The atomic ratio of Al to O in region I is about 2:2.7, giving a y value of 2.7. With increasing etching time, the intermixing layer containing Al_2O_y and TiO_x, which can be observed in region II, manifests a continuous change of the relative atomic ratios of Al, Ti, and O. Beneath region II is a more complex intermediate layer containing Al, Ti, Si, and O, marked as region III. The Si in region III should originate from the native SiO_2 layer on the surface of n^{++}-Si substrates. The total thickness of the bilayer Al_2O_y/TiO_x is estimated to be 45 nm (measured by AFM). The inset of Figure 2 shows the depth profiles of atomic composition obtained from a 12 nm thick, single layer TiO_x. There exists a transition layer consisting of TiO_x and native SiO_2 in the spin-coated TiO_x film, as noted by the changes in the composition of the film. Interestingly, as observed in both bilayer Al_2O_y/TiO_x and single layer TiO_x, the C atom percentage at the surface is high and then decreases drastically as the etching depth increases. The high C concentration at the surface is usually attributed to contamination during sample handling; on the other hand, the absence of C atoms in the inner part of the oxide layer reveals that the Ti precursor ($Ti(OC_3H_7)_4$) is also completely decomposed. In the case of single layer TiO_x, the atomic ratio of Ti and Si to O is smaller than 2, suggesting that some oxygen vacancies exist in the transition layer. The impact of these oxygen vacancies on the electrical properties of the oxide layer will be discussed later.

To characterize the electronic properties of the solution-processed dielectric, we fabricate an Au/metal-oxides/n^{++}-Si (MIM) sandwiched structure and test its current−voltage characteristics. Figure 3 shows the typical leakage current density versus bias voltage plots of a single layer TiO_x and bilayer Al_2O_y/TiO_x system. As can be seen from Figure 3, the single layer TiO_x exhibits an asymmetrical curve shape, with current density of $\sim 1 \times 10^{-5}$ A/cm^2 at -2 V and nearly 0.1 A/cm^2 at +2 V (electric field strength: ∼1.7 MV/cm). This is likely due to the zero conduction band offset at the Si/TiO_x interface[8] and the different work function of Si and Au, making electron injection from one electrode easier than the other. We also note that the dip of the leakage current is shifted away from the zero bias; this might be caused by the charge trapping at the defects (e.g., oxygen vacancies) within the amorphous TiO_x/SiO_2 transition layer. After deposition of the Al_2O_y layer, the leakage current was reduced by 4 orders of magnitude under positive bias of +2 V (electric field strength: ∼ 0.5 MV/cm). The reduction of leakage is due to the blocking of electron conduction path by the Al_2O_y layer. For both the single layer and bilayer devices we observe an abrupt slope change of the leakage current at high positive bias as indicated by the transition from region A to B as shown in Figure 3. Similar phenomenon has also been observed by Mahapatra et al.[18] and studied in detail. According to their analysis, the conduction in region A is governed by a charge hopping process and the conduction in region B is dominated by both Proole−Frenkel emission and trap assisted tunneling processes.[18] Detailed characterization and modeling of the voltage and temperature dependences of the leakage current is needed to verify if the above explanation fits our system, and will be carried out in our future work.

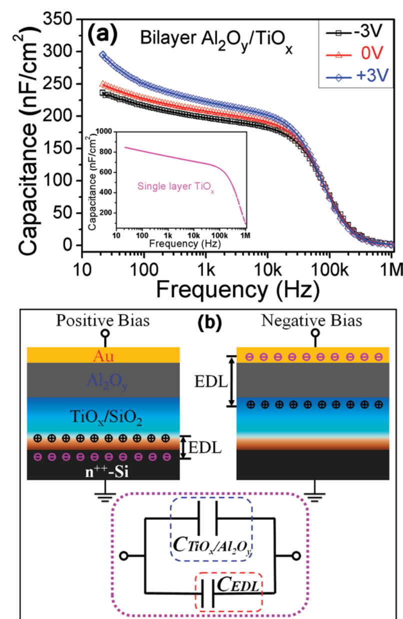


Figure 4. (a) Capacitance density versus frequency plots of MIM structures; (b) schematic view of the bilayer Al_2O_y/TiO_x capacitor and the equivalent circuit (lower part).

Figure 4a exhibits the frequency dependence of capacitance density for the Au/Al_2O_y/TiO_x /n^{++}-Si (MIM) structure measured under different bias voltages. The inset corresponds to that of the single layer TiO_x under 0 V bias. During the measurements, bias voltage is applied to the top Au electrode, while the bottom Si substrate is grounded. For single layer TiO_x, under a bias voltage of 0 V, the total capacitance density is ∼850 nF/cm^2 at 20 Hz. As shown in Figure 2, as the TiO_x/SiO_2 transition layer is present in the spin-coated film in the case of single layer TiO_x, it is appropriate to calculate the equivalent permittivity of this transition layer instead of that of TiO_x. Using the thickness value of 12 nm, an equivalent k value of about 12 can be extracted. As for the bilayer Al_2O_y/TiO_x, capacitance density is reduced owing to the introduction of another capacitor (i.e., Al_2O_y) in series. As can be seen in Figure 4a, application of a forward bias (biasing positively on the Au electrode) results in higher capacitance of the MIM structure, compared to zero or reverse bias. Similar bias dependent capacitance has been observed by Yarmarkin et al. in the Au/TiO_2/Pt resistive switching device.[19] They attribute this phenomenon to the variation of space charge distribution, i.e., the redistribution of oxygen vacancies in the film driven by the applied voltages. This may also explain our bilayer Al_2O_y/TiO_x

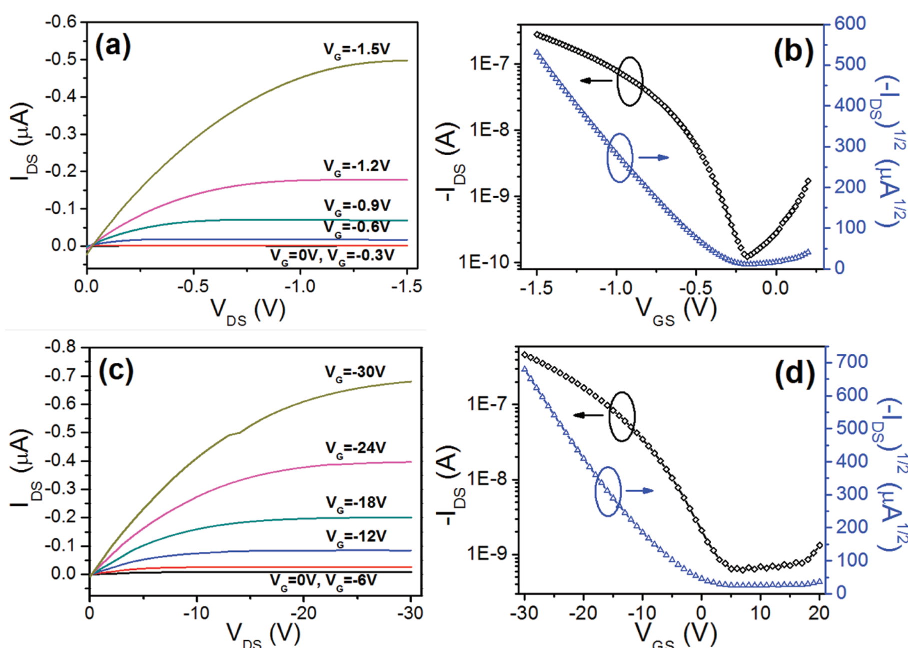


Figure 5. (a) Output curves (I_{DS} vs V_{DS}), (b) Transfer curve [$-I_{DS}$ vs V_{GS}, $(-I_{DS})^{1/2}$ vs V_{GS}] at a constant V_{DS} of -1.5 V of OFET using bilayer Al_2O_y/TiO_x as dielectric; (c) Output curves (I_{DS} vs V_{DS}), (d) Transfer curve [$-I_{DS}$ vs V_{GS}, $(-I_{DS})^{1/2}$ vs V_{GS}] at a constant V_{DS} of −30 V of OFET using traditional 300 nm SiO_2 as dielectric.

system, because our XPS results suggest the existence of oxygen vacancies in the vicinity of the TiO_x/SiO_2 transition layer. The oxygen vacancies in TiO_2 are known to be positively charged and mobile.[20] Having this in mind, one can infer that under forward bias, the oxygen vacancies will be repelled away from the mixing layer and accumulate close to the bottom Si substrate. This positively charged oxygen vacancy accumulation layer induces additional electrons at the bottom electrode, forming an "electric double-layer" (EDL) capacitor. The capacitance of such an EDL could be enlarged due to its thickness (a few nanometers).[21] On the other hand, in the situation of reverse bias, the oxygen vacancies will be attracted towards the Au electrode, and then blocked at Al_2O_y/TiO_x interface (as shown in Figure 4b), resulting in a larger thickness of the EDL capacitance. This explains the bias voltage dependence of the capacitance of bilayer Al_2O_y/TiO_x observed in Figure 4a. Similar results have also been reported by other groups.[22,23]

Besides the bias dependence, we also observe a slight increase of capacitance density at low frequencies. The increase of capacitance at low frequency is often related to the Maxwell—Wagner space charge polarization which is inherently a nonuniform charge accumulation.[24,25] This process is also referred to as electrode polarization according to Gonon et al.,[26] in which the mobile charges form an EDL against the electrodes resulting in a bias modulated EDL capacitance. As discussed previously, in the intermixing layer of bilayer Al_2O_y/TiO_x, oxygen vacancies are positively charged and mobile. Under an AC bias with sufficiently low frequencies, the oxygen vacancies will have enough time to respond to the bias change and go back and forth in the vicinity of the space charge layer, which can be viewed as a macroscopic dipole oscillating with the field. The lower the frequency, the larger the distance of oscillation, and ultimately the larger the capacitance density. To illustrate the mechanism for the voltage and frequency dependent capacitance, a simple model with an equivalent circuit is proposed in Figure 4b. To calculate the equivalent dielectric constant of the bilayer Al_2O_y/TiO_x, the low-frequency (20 Hz) capacitance value of 250 nF/cm^2 under zero bias is considered. Using the thickness of 45 nm, an equivalent dielectric constant of about 13.3 is expected.

To demonstrate the effectiveness of our bilayer Al_2O_y/TiO_x system, bottom-gate, top-contact (BGTC) CuPc FETs with gold source-drain electrodes are fabricated using the bilayer system as the gate dielectric. More than 5 bilayer Al_2O_y/TiO_x substrates are used, and 4 devices on each substrate are fabricated and tested. The device yield is about 90%. Figure 5a shows the output curves of a representative CuPc FET. Due to the high capacitance of our bilayer Al_2O_y/TiO_x system, the device can work effectively at operation voltages as low as −1.5 V. The output curves exhibit clear linear and saturation regions. Though moderate leakage current still exists at zero drain voltage, its magnitude is much smaller than the corresponding saturated channel current at respective gate voltages. Figure 5b shows the corresponding transfer curve in the saturation region and $(-I_{DS})^{1/2}$ versus V_{GS} plot. By using a linear fit of the plot in Figure 5b, we can determin V_T in the saturation region from the following equation

$$I_{DS} = \frac{W}{2L} C_i \mu (V_{GS} - V_T)^2$$

where W is the channel width, L is the channel length, V_T is the threshold voltage, μ is the hole mobility, and C_i is the capacitance density of the gate dielectric. To extract the hole mobility of CuPc FETs, we consider the C_i value of the bilayer Al_2O_y/TiO_x system under zero bias of 250 nF/cm^2 at 20 Hz. From Figure 5b, the hole mobility (μ), threshold voltage (V_T), on/off ratio, and subthreshold swing (SS) are determined to be 0.06 cm^2/(V s), −0.5 V, 2×10^3, and 160 mV/dec, respectively. Interestingly, the properties of the low-voltage CuPc FETs using bilayer Al_2O_y/TiO_x as the gate dielectric are better than those prepared on various high-k metal-oxide thin films, such as ZrO_2,[27] Al_2O_3, Ta_2O_5,[28] and HfO_2,[29] and even higher than the value reported by

Table 1. Summary of the Electric Performance of Bilayer Al_2O_y/TiO_x and 300 nm SiO_2 Gated CuPc OFETs

dielectric	electric performance			
	μ (cm²/(V s))	V_T (V)	on/off ration	SS (mV/dec)
Al_2O_y/TiO_x	0.06	−0.5	2×10^3	160
SiO_2	0.004	−5.1	1×10^3	6.7×10^3

Wang et al. (~0.04 cm²/(V s)),[30] which is the highest mobility for CuPc thin film transistors so far to the best of our knowledge. Noting that the capacitance density of the bilayer Al_2O_y/TiO_x system in steady−state condition is a little bit larger than that measured at 20 Hz (as inferred from Figure 4a), we may have overestimated our mobility by a factor of 1.5. As discussed previously, the low atomic scale roughness of our bilayer Al_2O_y/TiO_x may benefit charge carrier transport in the channel, resulting in improved performance. In addition, it is worth noting that a *SS* value of only 160 mV/dec is remarkably small. *SS* determines the voltage swing required for a transistor to turn from "off" to "on", and should be as low as possible, with a theoretical limit of about 60 mV/dec at room temperature.[31] Fabrication of OFETs with *SS* smaller than 180 mV/dec is thought to be a significant leap forward.[32,33]

In our low-voltage CuPc FETs, a gate voltage of −1.5 V can induce a hole density of 3.7×10^{-7} C/cm² in the channel, which is almost comparable to that of the OFETs made on conventional 300 nm SiO_2 (11 nF/cm²) operated at a gate voltage of −30 V. For comparison, we fabricate CuPc FETs on conventional 300 nm SiO_2 using the same processing condition. The corresponding electrical characteristics are shown in Figure 5c,d. Similar I_{DS} is obtained upon applying a −30 V gate voltage, as shown in Figure 5c. On the other hand, a relatively higher off-state current is also observed as compared to the low-voltage FETs. The high off-state current might be due to the high bulk conductance of CuPc caused by a complex charge-transfer reaction between O_2 and CuPc assited by moisture, and the high V_{DS} (−30 V).[34] The hole mobility (μ), threshold voltage (V_T), on/off ratio, and subthreshold swing estimated from Figure 5d are 0.004 cm²/(V s), −5.1 V, 1×10^3, and 6.7 V/dec, respectively. The electrical characteristics for both the bilayer Al_2O_y/TiO_x and 300 nm SiO_2 gated OFETs are summarized in Table 1. Interestingly, the mobility of the conventional 300 nm SiO_2-based OFET is much smaller than that of the bilayer Al_2O_y/TiO_x-based OFET. This could be due to the difference in the surface properties, e.g., roughness, surface energy and surface dipole, of the two gate dielectrics. A detailed study on the relation between these properties and the charge transport in CuPc is underway.

CONCLUSION

In summary, we have successfully achieved low-voltage OFETs by introducing a solution-processed, low-*T* cured high-*k* bilayer Al_2O_y/TiO_x system as the gate dielectric. The bilayer dielectric system exhibits a very smooth surface with RMS of about 0.22 nm, an equivalent *k* value of 13.3, a high capacitance of 250 nF/cm² and a low leakage current density of 1×10^{-5} A/cm². Upon using the high-*k* bilayer Al_2O_y/TiO_x as the gate dielectric, CuPc based OFETs exhibit hole mobility as high as 0.06 cm²/(V s) and *SS* value of only 160 mV/dec under an operation voltage as low as −1.5 V, and this performance is much better than that of devices obtained on conventional 300 nm SiO_2 substrates (0.004 cm²/(V s) and 6.7 V/dec for mobility and *SS* value, respectively). Our low-temperature, solution-processed method for fabrication of high-*k* gate dielectric provides a feasible approach to realize low-voltage circuits.

ASSOCIATED CONTENT

Supporting Information. X-ray diffraction (XRD) patterns of solution-processed single layer TiO_x and bilayer Al_2O_y/TiO_x system. This material is available free of charge via the Internet at http://pubs.acs.org.

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REFERENCES

(1) Liu, Z.; Oh, J. H.; Roberts, M. E.; Wei, P.; Paul, B. C.; Okajima, M.; Nishi, Y.; Bao, Z. *Appl. Phys. Lett.* **2009**, *94*, 203301.
(2) Coropceanu, V.; Cornil, J.; da Silva Filho, D. A.; Olivier, Y.; Silbey, R.; Brédas, J.-L. *Chem. Rev.* **2007**, *107*, 926–952.
(3) Dimitrakopoulos, C. D.; Malenfant, P. R. L. *Adv. Mater.* **2002**, *14*, 99–117.
(4) Klauk, H.; Zschieschang, U.; Pflaum, J.; Halik, M. *Nature* **2007**, *445*, 745–748.
(5) Yoon, M. H. *Proc. Natl. Acad. Sci. U.S.A.* **2005**, *102*, 4678–4682.
(6) Yan, H.; Chen, Z.; Zheng, Y.; Newman, C.; Quinn, J. R.; Dötz, F.; Kastler, M.; Facchetti, A. *Nature* **2009**, *457*, 679–686.
(7) Yoon, M. H.; Yan, H.; Facchetti, A.; Marks, T. J. *J. Am. Chem. Soc.* **2005**, *127*, 10388–10395.
(8) Robertson, J. *Eur. Phys. J. Appl. Phys.* **2004**, *28*, 265–291.
(9) Mikhelashvili, V.; Eisenstein, G. *Thin Solid Films* **2006**, *515*, 346–352.
(10) Dezelah, C. L.; Niinisto, J.; Kukli, K.; Munnik, F.; Lu, J.; Ritala, M.; Leskela, M.; Niinisto, L. *Chem. Vap. Deposition* **2008**, *14*, 358–365.
(11) Duenas, S.; Castan, H.; Garcia, H.; de Castro, A.; Bailon, L.; Kukli, K.; Aidla, A.; Aarik, J.; Mandar, H.; Uustare, T.; Lu, J.; Harsta, A. *J. Appl. Phys.* **2006**, *99*, 054902.
(12) Maunoury, C.; Dabertrand, K.; Martinez, E.; Saadoune, M.; Lafond, D.; Pierre, F.; Renault, O.; Lhostis, S.; Bailey, P.; Noakes, T. C. Q.; Jalabert, D. *J. Appl. Phys.* **2007**, *101*, 034112.
(13) Li, W.; Auciello, O.; Premnath, R. N.; Kabius, B. *Appl. Phys. Lett.* **2010**, *96*, 162907.
(14) Lee, J.; Kim, J. H.; Im, S. *Appl. Phys. Lett.* **2003**, *83*, 2689.
(15) Ramajothi, J.; Ochiai, S.; Kojima, K.; Mizutani, T. *Jpn. J. Appl. Phys.* **2008**, *47*, 8279–8283.
(16) Park, J.; Park, S. Y.; Shim, S. O.; Kang, H.; Lee, H. H. *Appl. Phys. Lett.* **2004**, *85*, 3283.
(17) Fritz, S. E.; Kelley, T. W.; Frisbie, C. D. *J. Phys. Chem. B* **2005**, *109*, 10574.
(18) Mahapatra, R.; Chakraborty, A. K.; Poolamai, N.; Horsfall, A.; Chattopadhyay, S.; Wright, N. G.; Coleman, K. S.; Coleman, P. G.; Burrows, C. P. *J. Vac. Sci. Technol., B* **2007**, *25*, 217–223.
(19) Yarmarkin, V. K.; Shul'man, S. G.; Lemanov, V. V. *Phys. Solid State* **2008**, *50*, 1841–1847.

(20) Weibel, A.; Bouchet, R.; Knauth, P. *Solid State Ionics* **2006**, *177*, 229–236.
(21) Gonon, P.; El Kamel, F. *Appl. Phys. Lett.* **2007**, *90*, 232902.
(22) Paskaleva, A.; Lemberger, M.; Bauer, A. J.; Weinreich, W.; Heitmann, J.; Erben, E.; Schroder, U.; Oberbeck, L. *J. Appl. Phys.* **2009**, *106*, 054107.
(23) El Kamel, F.; Gonon, P.; Vallee, C. *Appl. Phys. Lett.* **2007**, *91*, 172909.
(24) Blonkowski, S.; Regache, M.; Halimaoui, A. *J. Appl. Phys.* **2001**, *90*, 1501.
(25) Ramanathan, S.; Park, C. M.; McIntyre, P. C. *J. Appl. Phys.* **2002**, *91*, 4521.
(26) Gonon, P.; El Kamel, F. *J. Appl. Phys.* **2007**, *101*, 073901.
(27) Shang, L. W.; Liu, M.; Tu, D. Y.; Liu, G.; Liu, X. H.; Ji, Z. Y. *IEEE Trans. Electron Dev.* **2009**, *56*, 370–376.
(28) Higuchi, T.; Murayama, T.; Itoh, E.; Miyairi, K. *Thin Solid Films* **2006**, *499*, 374–379.
(29) Tang, W. M.; Helander, M. G.; Greiner, M. T.; Dong, G.; Ng, W. T.; Lu, Z. H. *IEEE International Conference of Electron Devices and Solid-State Circuits 2009*; Xi'an, China, Dec 25−27, 2009; IEEE: Piscataway, NJ, 2009; p 513
(30) Wang, J.; Wang, H. B.; Yan, X. J.; Huang, H. C.; Jin, D.; Shi, J. W.; Tang, Y. H.; Yan, D. H. *Adv. Funct. Mater.* **2006**, *16*, 824–830.
(31) Sze, S. M.; Ng, K. K. *Physics of Semiconductor Devices*, 3rd ed.; Wiley & Sons: Hoboken, NJ, 2007; pp 227−228.
(32) Jang, Y.; Kim, D. H.; Park, Y. D.; Cho, J. H.; Hwang, M.; Cho, K. *Appl. Phys. Lett.* **2006**, *88*, 072101.
(33) Majewski, L. A.; Schroeder, R.; Grell, M. *Adv. Mater.* **2005**, *17*, 192–196.
(34) Yan, X. J.; Wang, H.; Yan, D. H. *Thin Solid Films* **2006**, *515*, 2655–2658.